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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,761	06/19/2001	Kazunobu Kuwazawa	15.44/5852	4015

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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,761	KUWAZAWA, KAZUNOBU	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

Drawings

1. Figures 5 and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claim1-6, and 8-24 rejected under 35 U.S.C. 102(a) as being anticipated by Zhou et al. Patent Number 6156598.

Zhou discloses:

(See figures 1-5 col. 3 lines 49-51, 58-67; col. 4 lines 1-67; col. 5 lines 57-62)

> 1. A method for manufacturing a semiconductor device, the method comprising:
> (a) forming a gate dielectric layer (21) over a semiconductor substrate (11);
> (b) forming a gate electrode (22) over the gate dielectric layer;
> (c) forming an extension control layer (40A) over the semiconductor substrate on sides of
> the gate dielectric layer; and
> (d) forming a first impurity layer and a second impurity layer by ion-implanting an impurity in the semiconductor substrate,
> wherein an extension region (64) is formed in the semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer.

2. A method for manufacturing a semiconductor device according to claim 1, wherein the step (c) further includes the step of forming a sidewall protection film on sidewalls of the gate electrode with the extension control layers.

3. A method for manufacturing a semiconductor device according to claim 2, wherein the step (c) further includes the steps of:

(c - 1) forming a dielectric layer (21)over the semiconductor substrate;

(c - 2) forming a sidewall mask layer (50) on sides of the gate electrode over the dielectric layer;

(c - 3) removing the dielectric layer using the sidewall mask layer as a mask to form
the extension control layer and the sidewall protection layer; and

(c - 4) removing the sidewall mask layer after the step (c - 3).

4. A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon nitride.

5. A method for manufacturing a semiconductor device according to claim 4, wherein the sidewall mask layer is formed from a material comprising silicon oxide.

6. A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon oxide.

8. A method for manufacturing a semiconductor device according to claim 1, wherein the extension control layer has a thickness of 5 - 50 nm.

9. A method for manufacturing a semiconductor device according to claim 3, wherein the sidewall mask layer is formed to a thickness of 30 - 200 nm.

10. A semiconductor device comprising:

a gate dielectric layer provided over a semiconductor substrate;

a gate electrode provided over the gate dielectric layer;

a first impurity layer and a second impurity layer provided in the semiconductor substrate and spaced away from sides of the gate dielectric layer;

an extension region provided in the semiconductor substrate between the gate dielectric layer and at least one of the first impurity layer and the second impurity layer; and

an extension control layer provided over the extension region.

11. A semiconductor device according to claim 10, further comprising a sidewall
protection film formed on sidewalls of the gate electrode.

12. A semiconductor device according to claim 11, wherein the sidewall protection film comprises silicon oxide and the extension control layer comprises silicon nitride.

13. A semiconductor device according to claim 11, wherein the sidewall protection film comprises silicon nitride and the extension control layer comprises silicon oxide.

14. A semiconductor device according to claim 11, wherein the sidewall protection film is integral with the extension control layer.

15. A semiconductor device according to claim 11, wherein the extension control layer and the sidewall protection film define a substantially L-shaped cross-sectional configuration.

16. A semiconductor device according to claim 10, wherein the extension control layer comprises silicon nitride.

17. A semiconductor device according to claim 10, wherein the extension control layer comprises silicon oxide.

18. A semiconductor device according to claim 10, wherein the extension control layer has a thickness of 5 - 50 nm.

19. A semiconductor device according to claim 10, wherein the extension region includes portions provided in the semiconductor substrate between the gate dielectric layer and both the first impurity layer and the second impurity layer.

20. A semiconductor device according to claim 19, further comprising a sidewall protection film on sidewalls of the gate electrode, wherein the extension control layer and sidewall protection film form a substantially L-shaped structure in cross section on at least one side of the gate dielectric layer.

21. A method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer; and

a single ion-implanting step that forms extension regions in the semiconductor substrate under the extension control structures and source/drain regions in the semiconductor substrate adjacent to the extension layer, wherein the extension regions have a depth that is less than that of the source/drain regions.

22. A method according to claim 21, further comprising forming sidewall protection structures on sidewalk of the gate electrode, wherein the sidewall protection structures are formed from the same material as the extension control structures.

23. A method according to claim 22, wherein the extension control structures and sidewall protection structures are formed using a method comprising:

depositing a dielectric layer over the surface of the semiconductor substrate and gate electrode;

forming a mask layer on the dielectric layer;

anisotropically etching the mask layer to form a sidewall mask layer;

etching the dielectric layer using the sidewall mask layer as a mask so that the dielectric layer remains at sidewalk of the gate electrode and extends a distance outward from the gate dielectric layer along the surface of the dielectric layer; and

removing the sidewall mask layer;

wherein the dielectric layer remaining at sidewalls of the gate electrode defines the sidewall protection structures and the dielectric layer extending a distance outward gate dielectric layer along the surface of the dielectric layer defines the extension control structures.

24. A method of manufacturing a semiconductor device according to claim1, wherein the extension control layer is formed from a dielectric material.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. Patent Number 6156598, in further view of Akamatsu et al. Patent Number 6180472.

Zhou discloses all the limitations of claims 1-6 and 8-24, except the limitation of claim 7 where the sidewall mask is a formed of a material comprising of silicon nitride, in which Akamatsu discloses:

(See figure 2a-b col. 7 lines 10-15, lines 40-42)

A protective film (12) made of silicon nitride, which is used as a mask layer, and a first sidewall (12a) mask.

Therefore, it would be obvious to one of ordinary skill in the art that it is a matter of inventor's choice as to the material used as a mask layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
May 15, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800